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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/519,741	11/04/2005	Ludwig Dittmar	2002 P 09188 US	9239

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EXAMINER	
DINH, THU HUONG T	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 09/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/519,741	DITTMAR ET AL.	
	Examiner	Art Unit	
	Thu-Huong Dinh	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-29 and 31-35* is/are rejected.

7)☒ Claim(s) *30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 November 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

WALTER LINDSAY JR.
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/25/2006 and 4/26/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. Claims 21-23, 25-27, 29,31 and 33 are rejected under 35 U.S.C. 102(e) as being anticipated by Prior Art,Gruening-Von Schwerin et al. (U.S.2004/0206722 filed April 18, 2002).

The applied reference has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Prior Art, Gruening-Von Schwerin et al. teaches a semiconductor substrate (column 2 [0024]) providing a first contact hole (K1) in an insulating layer (column 3 [0026]); and filling the contact hole (K1) with contact material (60) (column 5 [0060]) so that the contact material is electrically connected to a line (column 4 and column 5 [0056]); wherein a hard mask (M1) that is used to pattern the contact hole (column 5 [0057]) is subsequently re-patterned (column 5 [0058]) to define a conductor line trench

(70) which is connected thereto (column 5 [0062]) (Claim 21). Preferably, the hard mask (M1) is made from polycrystalline silicon (column 4 [0055]) (Claim 22, 29) and further comprising patterning said hard mask by means of a dry etching process (column 5 [0059]) (Claims 23,31). Prior Art, Gruening-Von Schwerin et al. teaches depositing a liner on a surface of said contact hole (K1) and line prior to said step of filling holes with Tungsten (column 5 [0062]) (Claims 25, 27and 34) and the liner is selected from the group consisting of Ti and TiN (column 5 [0062]) (Claim 26).

In respect to Claim 28, Prior Art, Gruening-Von Schwerin et al. teaches a semiconductor substrate (column 2 [0024]) providing a first contact hole (K1) in an insulating layer (column 3 [0026]); wherein a hard mask (M1) that is used to pattern the contact hole (column 5 [0057]) is subsequently re-patterned (column 5 [0058]) to define a conductor line trench (70) which is connected thereto (column 5 [0062]). The second contact holes can be formed after the formation of the first contact holes, e.g. the second contact holes can be etched selectively with respect to the material already filled into the first contact holes (column 3 [0029]) and filling the contact hole (K1) with contact material (60) (column 5 [0060]) so that the contact material is electrically connected to a line (column 4 and column 5 [0056]).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 21-22, 27-28, 29 and 34 are rejected under 35 U.S.C. 102(b) as being anticipated by Wang et al. (U.S. 6372631 dated April 16, 2002).

In respect to Claim 21, Wang et al. teaches the etching of the first insulator layer (22) leaves a first opening (36) such as via hole (column 8, lines 34-36) and the via hole (36) is filled with conductive material (column 8, lines 39-40). In Figure 7, a photoresist layer (34) is patterned on the hard mask layer (32) and then to be etched into the second dielectric layer (30) (column 7, lines 42-45). The trench opening is created by etching the hard mask (32) and the second dielectric layer (30) (column 7, lines 43-45). Figure 9 shows the via (40) electrically connecting the underlying conductive layer (20) to the conductive line (42) formed in the trench (38) (column 8, lines 49-51). In respect to Claim 22 and 29, Wang et al. teaches the hard mask layer (32) may comprise silicon nitride (column 7, lines 37-39). In Figure 5, the depositing a liner (30) on a surface of said contact hole and line prior to said step of filling (column 6, lines 42-44) (Claim 25). In respect to Claims 27 and 34, Wang et al. discussed the conventional semiconductor devices typically filling the opening with a conductive material, such as tungsten (W) (column 1, lines 48-50). In respect to Claim 28, Wang et al. teaches the insulating layer (22) (column 6, lines 1-3); the hard mask (28) patterned to form the via hole (column 6, lines 26-30) that will eventually be etched into the first dielectric layer (24) that is formed on the first insulator layer (22) (column 6, lines 13-14); etching said via hole in said insulating layer (column 8, lines 23-25); re-patterning said hard mask (32) (column 7,lines 37-40, lines 56-58) to form said conductor trench (38) connected to said via hole (40) (column 8, lines 49-51) and etching the conductor trench in said insulating layer

(column 7, lines 29-31); and filling said contact hole (36) and said conductor trench (38) with a conductive material (column 8 ,lines 39-40) such that said conductive material in said conductor trench and said contact hole are electrically connected (column 2, lines 53-55).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

6. Claims 23-24 and 31-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (U.S. 6372631 filed April 16, 2002) as applied to claims 21 and 28 above, and further in view of Carey (U.S. 5,173,442 dated December 22, 1992).

Wang et al. teaches the structure as claimed and as described in the preceding paragraphs; however, Wang et al. lacks anticipation only in not explicitly the teaching of: 1)...further comprising patterning said hard mask by means of a dry etching process (Claims 23, 31); 2) ...wherein said dry etching process comprises using at least one of the group SF_6, HBr and He/O_2 (Claims 24, 32).

Carey teaches the Methods of Forming Channels and Vias in Insulating Layers. The channels extending partially through and vias extending completely through an insulation layer in an electrical interconnect such as a substrate can be formed in a relatively few steps with low cost etching and patterning techniques. In Figure 1a, a thin

blanket layer of metal is sputtered over the insulation layer as polyimide layer (14) to form hard mask (16), which after conventional patterning has openings to expose via regions (20) and channel region (22) (column 3, lines 44-50). As plasma etch (24) is applied hard mask (16) etches slowly (column 3, lines 59-60) and plasma etch (24) can comprise 90% O2 and 10% SF6 (column 4, lines 3). While dry etching with plasma etches is the preferred method of etching, other etching methods is suitable for selectively removing material from the insulating layer (column 4, lines 42-45).

It would be obvious to one of ordinary skill in the art, at the time of invention was made, to modify the structure shown in Wang et al. with Carey's teaching of forming vias in an insulation layer with the motivation of reducing cost in etching and patterning techniques.

7. Claims 26,33 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (U.S. 6372631 filed April 16, 2002) as applied to claims 21 and 28 above, and further in view of Matsuoka et al. (U.S. 613049 filed October 10, 2000).

Wang et al. teaches the structure as claimed and as described in the preceding paragraphs; however, Wang et al. lacks anticipation only in not explicitly the teaching of: 1) ...wherein said liner is selected from the group consisting of Ti and TiN (Claim 26); 2)...further comprising the step of depositing a liner on a surface of said contact hole and conductor trench prior to said step of filling (Claim 33); 3)...wherein said liner is selected from the group consisting of Ti and TiN (Claim 35).

Matsuoka et al. teaches Semiconductor Memory Device and a Method for Fabricating the Same. To achieve a memory cell on a smaller scale, the three-

dimensional structure of a capacitor has been adopted in generations after the fourth generation in order to secure a larger capacitance in a smaller area. In the photolithography step, the depth of focus becomes smaller as the resolution is increased in order to achieve a finer pattern. Thus, the linewidth being a key element in a technology of miniaturization to be employed in the next generation of memory devices. In Figure 13, a silicon oxide film (901) is formed as an interlayer insulating film in such manner that the silicon oxide film (901) may cover the bitlines (601A) and interconnect metallization (610B). Contact hole for the storage nodes are further formed in the silicon oxide film (901) and TiN plug (502) (Figure 17) is formed in a contact hole for a storage node (column 7, lines 17-26). In Figure 3, a shallow trench isolation region (2) is formed on a main surface of the substrate (1) (column 8, lines 54-56) and depositing a silicon oxide film with a thickness of about 0.4 microns by means of a known CVD method; selective polishing off the oxide film formed on a region other than the trenches (column 8, lines 59-63). In Figure 17, TiN (502) was deposited on the surface with openings of the contact holes (1001) by means of CVD (column 10, lines 41-43).

It would be obvious to one of ordinary skill in the art, at the time of invention was made, to modify the structure shown in Wang et al. with Matsuoka et al. teaching of forming a dynamic random access memory device which is suitable for a higher integration complexity.

Allowable Subject Matter

8. Claim 30 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter: the prior art, either singly or in combination fails to anticipate or render obvious, the limitations of:

...further comprising covering said insulating layer with an ARC layer to fill said contact hole prior to said step of re-patterning said hard mask (Claim 30).

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

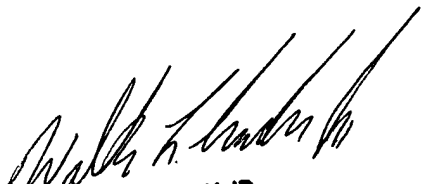
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thu-Huong Dinh whose telephone number is 571 272-9014. The examiner can normally be reached on Monday through Friday (8:30AM-5:00PM Eastern).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

thd



WALTER LINDSAY JR.
PRIMARY EXAMINER